7–1 THE JFET

The JFET (junction field-effect transistor) is a type of FET that operates with a reverse-biased *pn* junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, *n* channel or *p* channel.

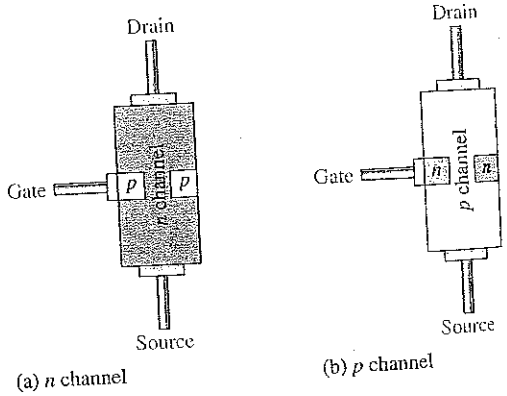
After completing this section, you should be able to

- **Explain the operation of JFETs**
- Identify the three terminals of a JFET
- Explain what a channel is
- Describe the structural difference between an *n*-channel JFET and a *p*-channel JFET
- Discuss how voltage controls the current in a JFET
- Identify the symbols for *n*-channel and *p*-channel JFETs

Figure 7–1(a) shows the basic structure of an *n*-channel **JFET** (junction field-effect transistor). Wire leads are connected to each end of the *n*-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a **channel**, and both *p*-type regions are connected to the **gate** lead. For simplicity, the gate lead is shown connected to only one of the *p* regions. A *p*-channel JFET is shown in Figure 7–1(b).

FIGURE 7–1

A representation of the basic structure of the two types of JFET.



Basic Operation

To illustrate the operation of a JFET, Figure 7–2 shows dc bias voltages applied to an *n* channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

The JFET is always operated with the gate-source pn junction reverse-biased. Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the *pn* junction, which extends into the *n* channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D. Figure 7–3 illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source. We will discuss JFET characteristic curves and some important parameters in Section 7–2.

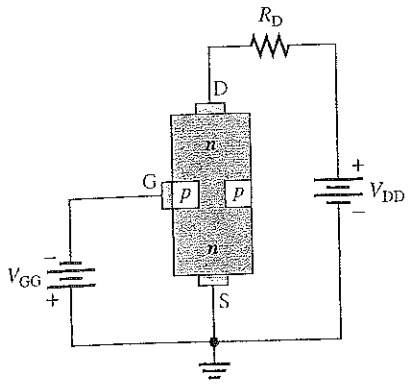
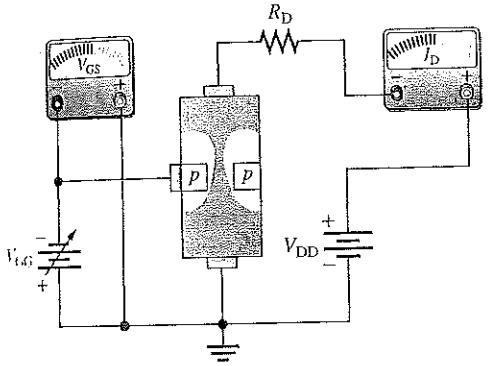
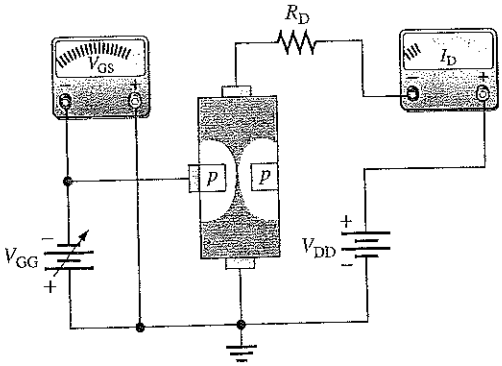


FIGURE 7–2

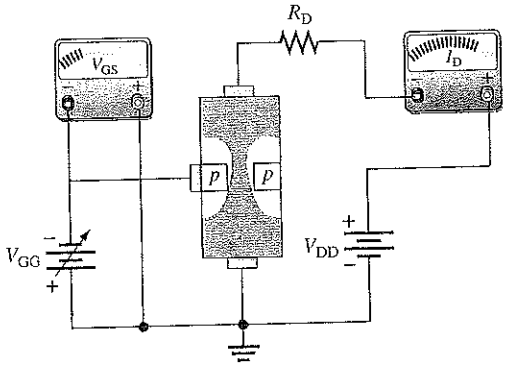
A biased *n*-channel JFET.



(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.



(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

FIGURE 7–3

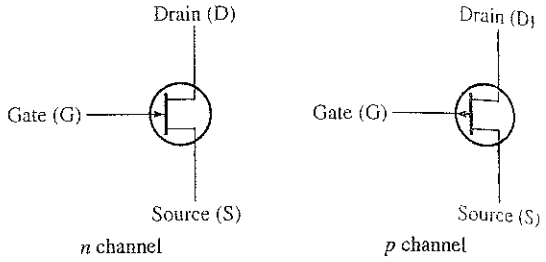
Effects of V_{GS} on channel width, resistance, and drain current ($V_{GG} = V_{GS}$).

JFET Symbols

The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure 7–4. Notice that the arrow on the gate points "in" for *n* channel and "out" for *p* channel.

FIGURE 7–4

JFET schematic symbols.



SECTION 7–1 REVIEW

Answers are at the end of the chapter.

1. Name the three terminals of a JFET.
2. Does an *n*-channel JFET require a positive or negative value for V_{GS}?
3. How is the drain current controlled in a JFET?

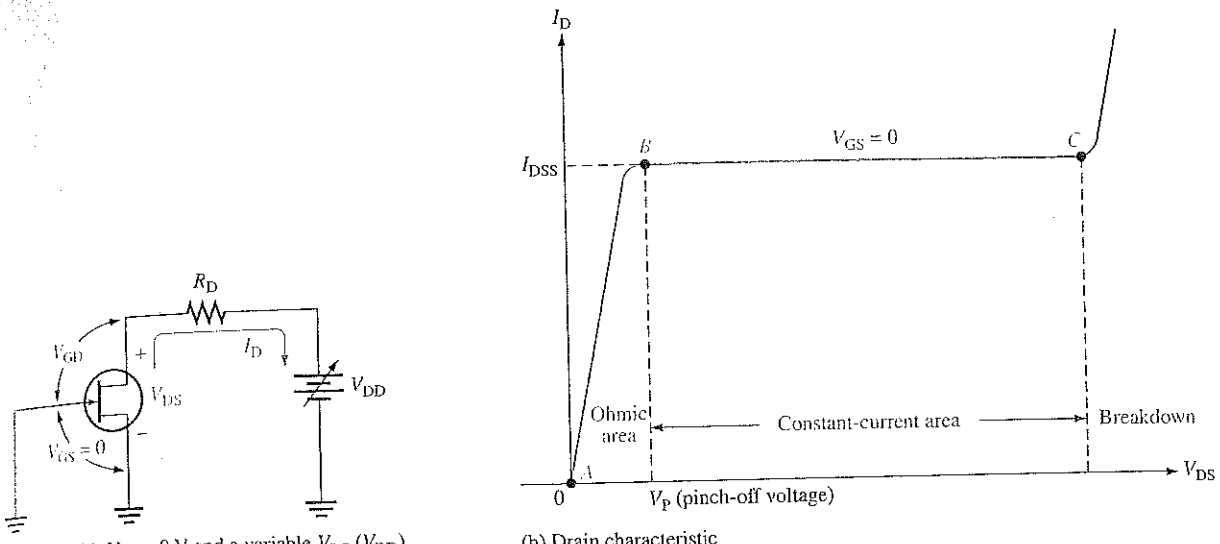
7–2 JFET CHARACTERISTICS AND PARAMETERS

In this section, you will see how the JFET operates as a voltage-controlled, constant-current device. You will also learn about cutoff and pinch-off as well as JFET transfer characteristics.

After completing this section, you should be able to

- **Define, discuss, and apply important JFET parameters**
- Explain ohmic area, constant-current area, and breakdown
- Define *pinch-off voltage*
- Describe how gate-to-source voltage controls the drain current
- Define *cutoff voltage*
- Compare pinch-off and cutoff
- Analyze a JFET transfer characteristic curve
- Use the equation for the transfer characteristic to calculate I_D
- Use a JFET data sheet
- Define *transconductance*
- Explain and determine input resistance and capacitance
- Determine drain-to-source resistance

Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0$ V). This is produced by shorting the gate to the source, as in Figure 7–5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 7–5(b) between points *A* and *B*. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic area because V_{DS} and I_D are related by Ohm's law.



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

FIGURE 7–5

The drain characteristic curve of a JFET for $V_{GS} = 0$ showing pinch-off.

At point B in Figure 7–5(b), the curve levels off and I_D becomes essentially constant. As V_{DS} increases from point B to point C, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

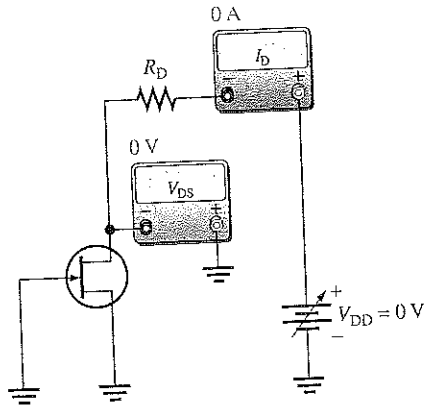
Pinch-Off Voltage

For $V_{GS} = 0$ V, the value of V_{DS} at which I_D becomes essentially constant (point B on the curve in Figure 7–5(b)) is the **pinch-off voltage**, V_P. For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET data sheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0$ V.

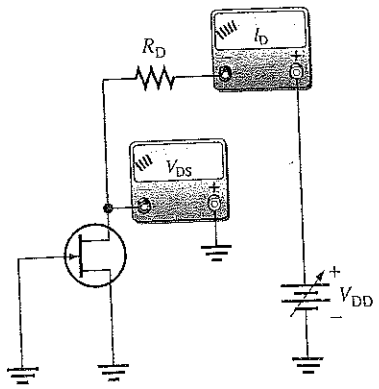
As shown in the graph in Figure 7–5(b), **breakdown** occurs at point C when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the constant-current area (between points B and C on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for $V_{GS} = 0$ V is illustrated in Figure 7–6.

V_{GS} Controls I_D

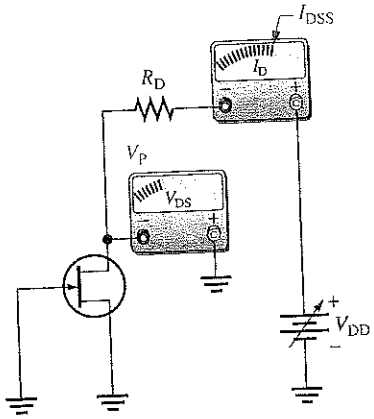
Let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure 7–7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure 7–7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P. Therefore, the amount of drain current is controlled by V_{GS}, as illustrated in Figure 7–8.



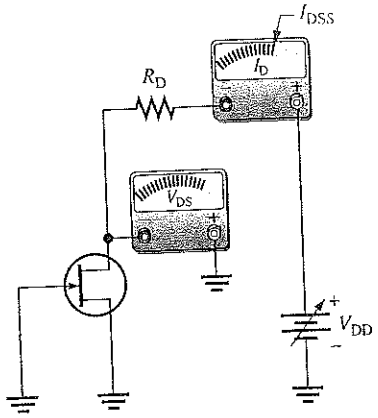
(a) When $V_{DS} = 0$, $I_D = 0$.



(b) I_D increases proportionally with V_{DS} in the ohmic area.



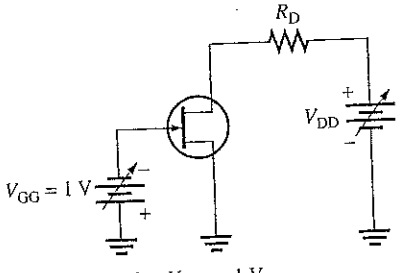
(c) When $V_{DS} = V_P$, I_D is consistant and equal to I_{DSS}.



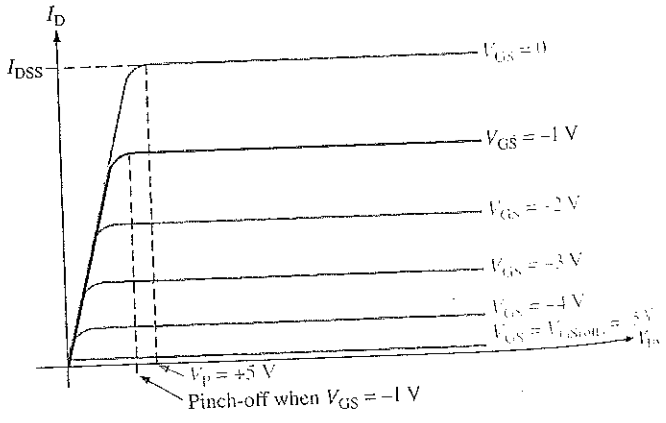
(d) As V_{DS} increases further, I_D remains at I_{DSS} until breakdown occurs.

FIGURE 7–6

JFET action that produces the characteristic curve for $V_{GS} = 0$ V.



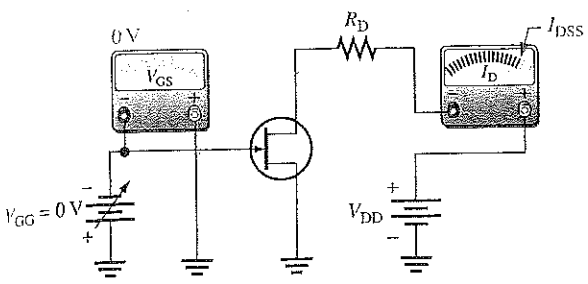
(a) JFET biased at $V_{GS} = -1$ V



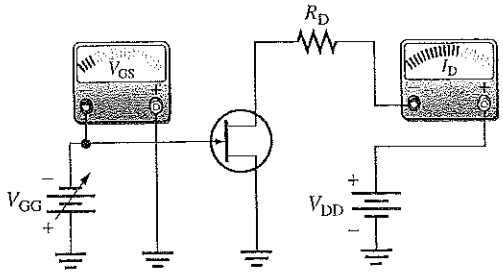
(b) Family of drain characteristic curves

FIGURE 7–7

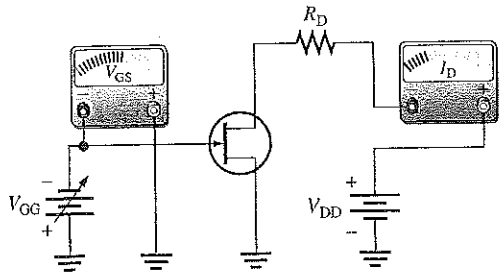
Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.



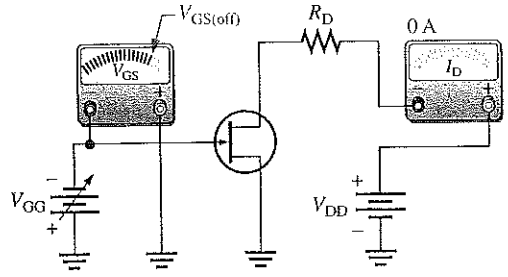
(a) $V_{GS} = 0$ V, $V_{DS} \geq V_P$, $I_D = I_{DSS}$



(b) When V_{GS} is negative, I_D decreases and is constant above pinch-off, which is less than V_P.



(c) As V_{GS} is made more negative, I_D continues to decrease but is constant above pinch-off, which has also decreased.



(d) Until $V_{GS} = -V_{GS(off)}$, I_D continues to decrease. When $V_{GS} \geq -V_{GS(off)}$, $I_D \cong 0$.

FIGURE 7–8

V_{GS} controls I_D.

Cutoff Voltage

The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage**, $V_{GS(off)}$. The JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

As you have seen, for an *n*-channel JFET, the more negative V_{GS} is, the smaller I_D becomes in the constant-current area. When V_{GS} has a sufficiently large negative value, I_D is reduced to zero. This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel, as shown in Figure 7–9.

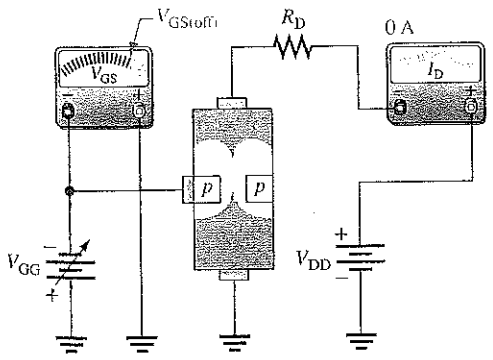


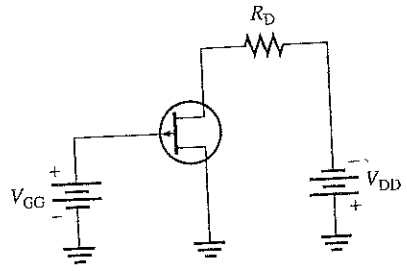
FIGURE 7–9

JFET at cutoff.

The basic operation of a *p*-channel JFET is the same as for an *n*-channel device except that a *p*-channel JFET requires a negative V_{DD} and a positive V_{GS}, as illustrated in Figure 7–10.

FIGURE 7–10

A biased *p*-channel JFET.



Comparison of Pinch-Off and Cutoff

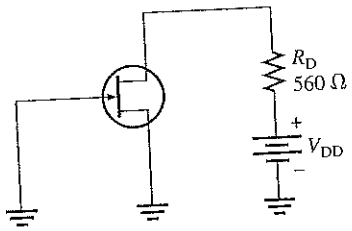
As you have seen, there is a difference between pinch-off and cutoff. There is also a connection. V_P is the value of V_{DS} at which the drain current becomes constant and is always measured at $V_{GS} = 0$ V. However, pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes constant varies with V_{GS}.

$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in sign. A data sheet usually will give either $V_{GS(off)}$ or V_P, but not both. However, when you know one, you have the other. For example, if $V_{GS(off)} = -5$ V, then $V_P = +5$ V, as shown in Figure 7–7(b).

EXAMPLE 7–1

For the JFET in Figure 7–11, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the *minimum* value of V_{DD} required to put the device in the constant-current area of operation.

FIGURE 7–11



Solution Since $V_{GS(off)} = -4$ V, $V_P = 4$ V. The minimum value of V_{DS} for the JFET to be in its constant-current area is

$$V_{DS} = V_P = 4 \text{ V}$$

In the constant-current area with $V_{GS} = 0$ V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12 \text{ mA})(560\ \Omega) = 6.72 \text{ V}$$

Apply Kirchhoff's law around the drain circuit,

$$V_{DD} = V_{DS} + V_{R_D} = 4 \text{ V} + 6.72 \text{ V} = \mathbf{10.7\ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current area.

*Related Problem** If V_{DD} is increased to 15 V, what is the drain current?

*Answers are at the end of the chapter.

EXAMPLE 7–2

A particular *p*-channel JFET has a $V_{GS(off)} = +4$ V. What is I_D when $V_{GS} = +6$ V?

Solution The *p*-channel JFET requires a positive gate-to-source voltage. The more positive the voltage, the less the drain current. When $V_{GS} = 4$ V, $I_D = 0$. Any further increase in V_{GS} keeps the JFET cut off, so I_D remains **0**.

Related Problem What is V_P for the JFET described in this example?

JFET Transfer Characteristic

You have learned that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an *n*-channel JFET, $V_{GS(off)}$ is negative, and for a *p*-channel JFET, $V_{GS(off)}$ is positive. Because V_{GS} does control I_D, the relationship between these two quantities is very important. Figure 7–12 is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D.

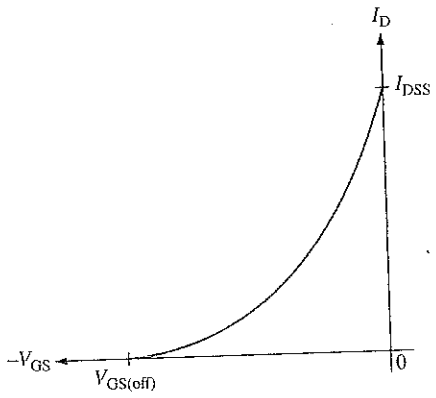


FIGURE 7–12
JFET transfer characteristic curve (*n*-channel).

Notice that the bottom end of the curve is at a point on the V_{GS} axis equal to $V_{GS(off)}$, and the top end of the curve is at a point on the I_D axis equal to I_{DSS}. This curve, of course, shows that the operating limits of a JFET are

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(off)}$$

and

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

The transfer characteristic curve can be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off, as illustrated in Figure 7–13 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves. For

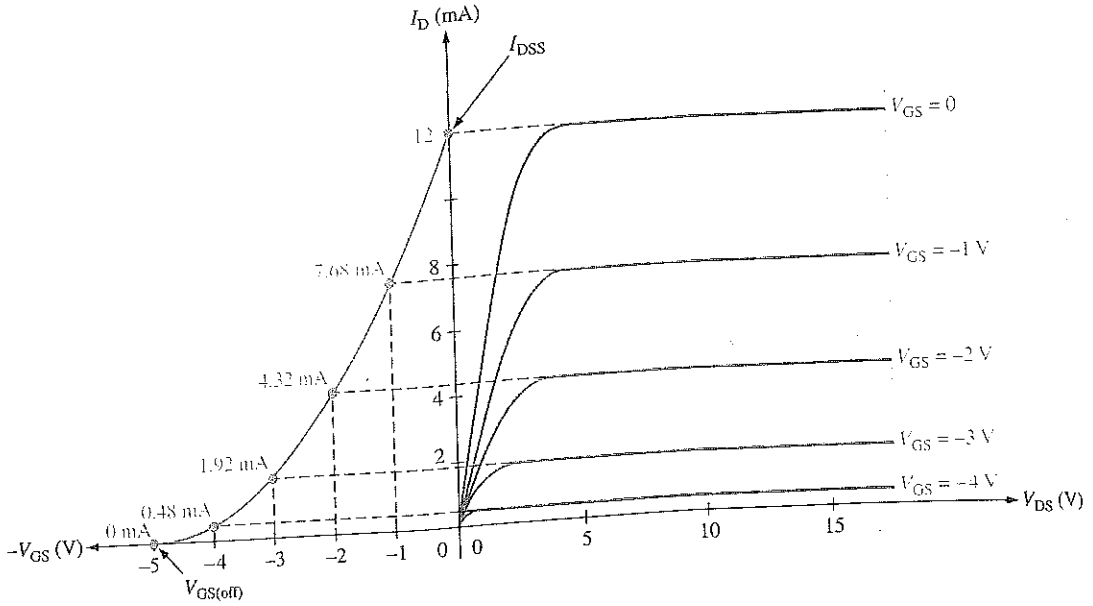


FIGURE 7–13
Example of the development of an *n*-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

example, when $V_{GS} = -2$ V, $I_D = 4.32$ mA. Also, for this specific JFET, $V_{GS(off)} = -5$ V and $I_{DSS} = 12$ mA.

A JFET transfer characteristic curve is expressed as

Equation 7–1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

With Equation 7–1, I_D can be determined for any V_{GS} if $V_{GS(off)}$ and I_{DSS} are known. These quantities are usually available from the data sheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a *square law*, and therefore, JFETs and MOSFETs are often referred to as *square-law devices*.

The data sheet for a typical JFET series is shown in Figure 7–14.

EXAMPLE 7–3

The partial data sheet in Figure 7–14 for a 2N5459 JFET indicates that typically $I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Using these values, determine the drain current for $V_{GS} = 0$ V, -1 V, and -4 V.

Solution For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\ mA}$$

For $V_{GS} = -1$ V, use Equation 7–1.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$
$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

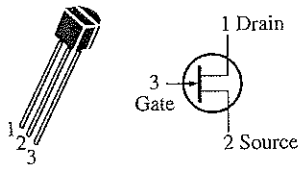
For $V_{GS} = -4$ V,

$$I_D = (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\text{ mA}}$$

Related Problem Determine I_D for $V_{GS} = -3$ V for the 2N5459 JFET.

2N5457
thru
2N5459

Case 29-04, Style 5
TO-92 (TO-226AA)



JFETs
General-Purpose

***N* channel — Depletion**

Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	25	V dc
Drain-Gate voltage	V_{DG}	25	V dc
Reverse gate-source voltage	V_{GSR}	–25	V dc
Gate current	I_G	10	mA dc
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction temperature	T_J	125	°C
Storage channel temperature range	T_{stg}	–65 to +150	°C

Electrical Characteristics ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF Characteristics						
Gate-Source breakdown voltage ($I_G = -10$ μA dc, $V_{DS} = 0$)		$V_{(BR)GSS}$	–25	–	–	V dc
Gate reverse current ($V_{GS} = -15$ V dc, $V_{DS} = 0$) ($V_{GS} = -15$ V dc, $V_{DS} = 0$, $T_A = 100°C$)		I_{GSS}	– –	– –	–1.0 –200	nA dc
Gate-Source cutoff voltage ($V_{DS} = 15$ V dc, $I_D = 10$ nA dc)	2N5457 2N5458 2N5459	$V_{GS(off)}$	–0.5 –1.0 –2.0	– – –	–6.0 –7.0 –8.0	V dc
Gate-Source voltage ($V_{DS} = 15$ V dc, $I_D = 100$ μA dc) ($V_{DS} = 15$ V dc, $I_D = 200$ μA dc) ($V_{DS} = 15$ V dc, $I_D = 400$ μA dc)	2N5457 2N5458 2N5459	V_{GS}	– – –	–2.5 –3.5 –4.5	– – –	V dc
ON Characteristics						
Zero-Gate-Voltage drain current ($V_{DS} = 15$ V dc, $V_{GS} = 0$)	2N5457 2N5458 2N5459	I_{DSS}	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mA dc
Small-signal Characteristics						
Forward transfer admittance common source ($V_{DS} = 15$ V dc, $V_{GS} = 0$, $f = 1.0$ kHz)	2N5457 2N5458 2N5459	$\lvert y_{fs} \rvert$	1000 1500 2000	– – –	5000 5500 6000	μmhos or μS
Output admittance common source ($V_{DS} = 15$ V dc, $V_{GS} = 0$, $f = 1.0$ kHz)		$\lvert y_{os} \rvert$	–	10	50	μmhos or μS
Input capacitance ($V_{DS} = 15$ V dc, $V_{GS} = 0$, $f = 1.0$ MHz)		C_{iss}	–	4.5	7.0	pF
Reverse transfer capacitance ($V_{DS} = 15$ V dc, $V_{GS} = 0$, $f = 1.0$ MHz)		C_{rss}	–	1.5	3.0	pF

FIGURE 7–14

JFET partial data sheet.

JFET Forward Transconductance

The forward **transconductance** (transfer conductance), g_m, is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

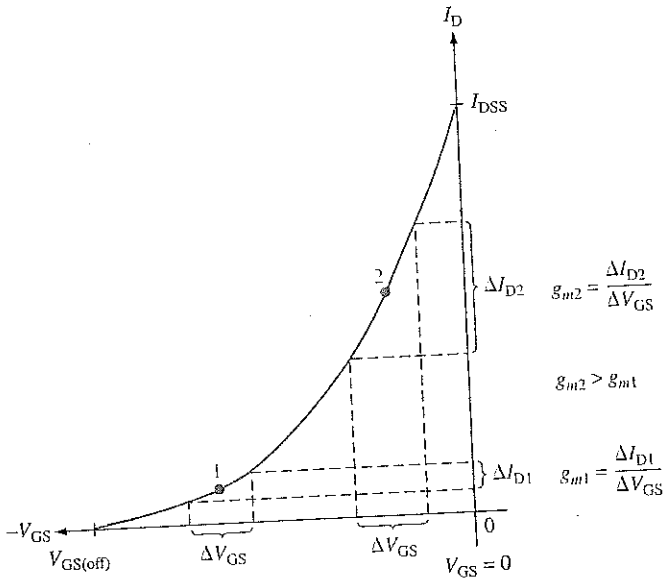
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are g_{fs} and y_{fs} (forward transfer admittance). As you will see in Chapter 8, g_m is important in FET amplifiers as a major factor in determining the voltage gain.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by V_{GS}. The value for g_m is greater near the top of the curve (near $V_{GS} = 0$) than it is near the bottom (near $V_{GS(off)}$), as illustrated in Figure 7–15.

FIGURE 7–15

g_m varies depending on the bias point (V_{GS}).



A data sheet normally gives the value of g_m measured at $V_{GS} = 0$ V (g_{m0}). For example, the data sheet for the 2N5457 JFET specifies a minimum g_{m0} (y_{fs}) of 1000 S with $V_{DS} = 15$ V.

Given g_{m0}, you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

Equation 7–2

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

When a value of g_{m0} is not available, you can calculate it using values of I_{DSS} and $V_{GS(off)}$. The vertical lines indicate an absolute value (no sign).

Equation 7–3

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

EXAMPLE 7–4

The following information is included on the data sheet in Figure 7–14 for a 2N5457 JFET: typically, $I_{DSS} = 3.0$ mA, $V_{GS(off)} = -6$ V maximum, and $y_{fs(max)} = 5000$ μS. Using these values, determine the forward transconductance for $V_{GS} = -4$ V, and find I_D at this point.

Solution $g_{m0} = y_{fs} = 5000\ \mu\text{S}$. Use Equation 7–2 to calculate g_m.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = (5000\ \mu\text{S})\left(1 - \frac{-4\text{ V}}{-6\text{ V}}\right) = \mathbf{1667\ \mu S}$$

Next, use Equation 7–1 to calculate I_D at $V_{GS} = -4$ V.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (3.0\text{ mA})\left(1 - \frac{-4\text{ V}}{-6\text{ V}}\right)^2 = \mathbf{333\ \mu A}$$

Related Problem A given JFET has the following characteristics: $I_{DSS} = 12$ mA, $V_{GS(off)} = -5$ V, and $g_{m0} = 3000\ \mu$S. Find g_m and I_D when $V_{GS} = -2$ V.

Input Resistance and Capacitance

As you know, a JFET operates with its gate-source junction reverse-biased, which makes the input resistance at the gate very high. This high input resistance is one advantage of the JFET over the BJT. (Recall that a bipolar junction transistor operates with a forward-biased base-emitter junction.) JFET data sheets often specify the input resistance by giving a value for the gate reverse current, I_{GSS}, at a certain gate-to-source voltage. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value (no sign):

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

For example, the 2N5457 data sheet in Figure 7–14 lists a maximum I_{GSS} of -1.0 nA for $V_{GS} = -15$ V at 25°C. I_{GSS} increases with temperature, so the input resistance decreases.

The input capacitance, C_{iss}, is a result of the JFET operating with a reverse-biased *pn* junction. Recall that a reverse-biased *pn* junction acts as a capacitor whose capacitance depends on the amount of reverse voltage. For example, the 2N5457 has a maximum C_{iss} of 7 pF for $V_{GS} = 0$.

EXAMPLE 7–5

A certain JFET has an I_{GSS} of -2 nA for $V_{GS} = -20$ V. Determine the input resistance.

Solution

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{20\text{ V}}{2\text{ nA}} = \mathbf{10{,}000\ M\Omega}$$

Related Problem Determine the minimum input resistance for the 2N5458 from the data sheet in Figure 7–14.

Drain-to-Source Resistance

You learned from the drain characteristic curve that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a large change in V_{DS} produces only a very small change in I_D. The ratio of these changes is the drain-to-source resistance of the device, r'_{ds}.

$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

Data sheets often specify this parameter in terms of the output conductance, g_{os}, or output admittance, y_{os}.

SECTION 7–2 REVIEW

1. The drain-to-source voltage at the pinch-off point of a particular JFET is 7 V. If the gate-to-source voltage is zero, what is V_P?
2. The V_{GS} of a certain *n*-channel JFET is increased negatively. Does the drain current increase or decrease?
3. What value must V_{GS} have to produce cutoff in a *p*-channel JFET with a $V_P = -3$ V?

7–3 JFET BIASING

Using some of the FET parameters discussed in the previous sections, you will now see how to dc-bias JFETs. Just as with the BJT, the purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. You will learn about two types of bias circuits, self-bias and voltage-divider bias.

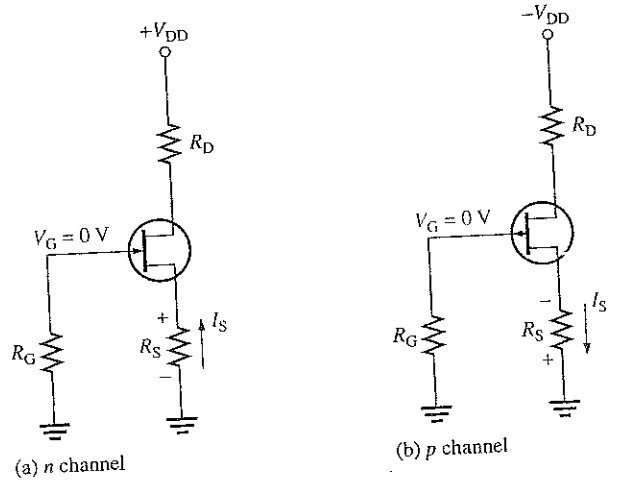
After completing this section, you should be able to

- **Discuss and analyze JFET bias circuits**
- Describe self-bias
- Analyze a self-biased JFET circuit
- Set the self-biased Q-point
- Analyze a JFET circuit with voltage-divider bias
- Use transfer characteristic curves to analyze JFET bias circuits
- Discuss Q-point stability

Self-Bias

Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an *n*-channel JFET and a positive V_{GS} for a *p*-channel JFET. This can be achieved using the self-bias arrangements shown in Figure 7–16. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an ac signal from ground in amplifier applications, as you will see later.

FIGURE 7–16
Self-biased JFETs ($I_S = I_D$ in all FETs).



For the *n*-channel JFET in Figure 7–16(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_D R_S$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Thus,

$$V_{GS} = -I_D R_S$$

For the *p*-channel JFET shown in Figure 7–16(b), the current through R_S produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since $I_S = I_D$,

$$V_{GS} = +I_D R_S$$

In the following analysis, the *n*-channel JFET in Figure 7–16(a) is used for illustration. Keep in mind that analysis of the *p*-channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

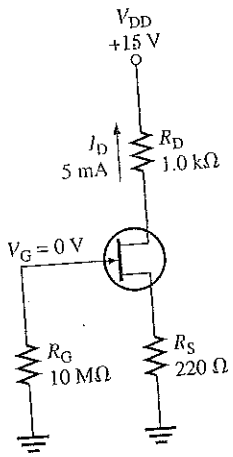
Since $V_S = I_D R_S$, the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$$

EXAMPLE 7–6

Find V_{DS} and V_{GS} in Figure 7–17. For the particular JFET in this circuit, the internal parameter values such as g_m, $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced. Another JFET, even of the same type, may not produce the same results when connected in this circuit due to the variations in parameter values.

FIGURE 7–17



Solution

$$V_S = I_D R_S = (5\text{ mA})(220\ \Omega) = 1.1\text{ V}$$

$$V_D = V_{DD} - I_D R_D = 15\text{ V} - (5\text{ mA})(1.0\text{ k}\Omega) = 15\text{ V} - 5\text{ V} = 10\text{ V}$$

Therefore,

$$V_{DS} = V_D - V_S = 10\text{ V} - 1.1\text{ V} = \mathbf{8.9\text{ V}}$$

Since $V_G = 0$ V,

$$V_{GS} = V_G - V_S = 0\text{ V} - 1.1\text{ V} = \mathbf{-1.1\text{ V}}$$

Related Problem Determine V_{DS} and V_{GS} in Figure 7–17 when $I_D = 8$ mA. Assume that $R_D = 860\ \Omega$, $R_S = 390\ \Omega$, and $V_{DD} = 12$ V.

Open the Multisim file E07-06 in the Examples folder on your CD-ROM. Measure I_D, V_{GS}, and V_{DS} and compare to the calculated values from the Related Problem.

Setting the Q-Point of a Self-Biased JFET

The basic approach to establishing a JFET bias point is to determine I_D for a desired value of V_{GS} or vice versa. Then calculate the required value of R_S using the following relationship. The vertical lines indicate an absolute value.

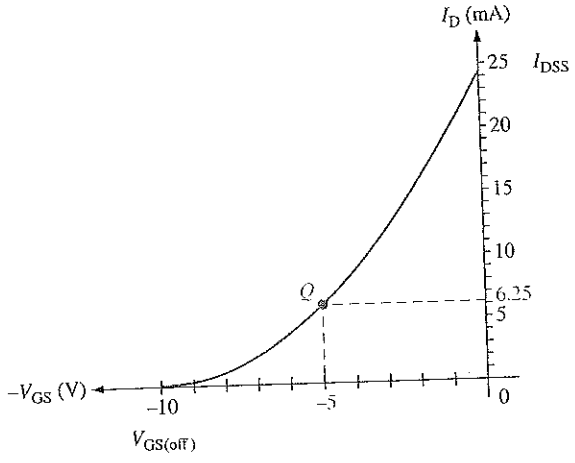
$$R_S = \left| \frac{V_{GS}}{I_D} \right|$$

For a desired value of V_{GS}, I_D can be determined in either of two ways: from the transfer characteristic curve for the particular JFET or, more practically, from Equation 7–1 using I_{DSS} and $V_{GS(off)}$ from the JFET data sheet. The next two examples illustrate these procedures.

EXAMPLE 7–7

Determine the value of R_S required to self-bias an *n*-channel JFET that has the transfer characteristic curve shown in Figure 7–18 at $V_{GS} = -5$ V.

FIGURE 7–18



Solution From the graph, $I_D = 6.25$ mA when $V_{GS} = -5$ V. Calculate R_S.

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5\ \text{V}}{6.25\ \text{mA}} = \mathbf{800\ \Omega}$$

Related Problem Find R_S for $V_{GS} = -3$ V.

EXAMPLE 7–8

Determine the value of R_S required to self-bias a *p*-channel JFET with $I_{DSS} = 25$ mA and $V_{GS(off)} = 15$ V. V_{GS} is to be 5 V.

Solution Use Equation 7–1 to calculate I_D.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (25\text{ mA})\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2$$
$$= (25\text{ mA})(1 - 0.333)^2 = 11.1\text{ mA}$$

Now, determine R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

Related Problem Find the value of R_S required to self-bias a *p*-channel JFET with $I_{DSS} = 18$ mA and $V_{GS(off)} = 8$ V. $V_{GS} = 4$ V.

Midpoint Bias It is usually desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. Under signal conditions, midpoint bias allows the maximum amount of drain current swing between I_{DSS} and 0. Using Equation 7–1, it is shown in Appendix B that I_D is approximately one-half of I_{DSS} when $V_{GS} = V_{GS(off)}/3.4$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS(off)}/3.4}{V_{GS(off)}}\right)^2 = 0.5I_{DSS}$$

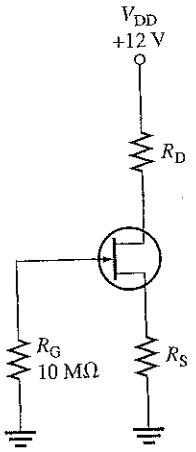
So, by selecting $V_{GS} = V_{GS(off)}/3.4$, you should get a midpoint bias in terms of I_D.

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop. Choose R_G arbitrarily large to prevent loading on the driving stage in a cascaded amplifier arrangement. Example 7–9 illustrates these concepts.

EXAMPLE 7–9

Select resistor values for R_D and R_S in Figure 7–19 to set up an approximate midpoint bias. For this particular JFET, the parameters are $I_{DSS} = 12$ mA and $V_{GS(off)} = -3$ V. V_D should be approximately 6 V (one-half of V_{DD}).

FIGURE 7–19



Solution For midpoint bias,

$$I_D \cong \frac{I_{DSS}}{2} = 6\text{ mA}$$

and

$$V_{GS} \cong \frac{V_{GS(off)}}{3.4} = \frac{-3\text{ V}}{3.4} = -882\text{ mV}$$

Then

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{882\text{ mV}}{6\text{ mA}} = \mathbf{147\ \Omega}$$

$$V_D = V_{DD} - I_D R_D$$

$$I_D R_D = V_{DD} - V_D$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{ V} - 6\text{ V}}{6\text{ mA}} = \mathbf{1\ k\Omega}$$

Related Problem Select resistor values in Figure 7–19 to set up an approximate midpoint bias. The JFET parameters are $I_{DSS} = 10$ mA and $V_{GS(off)} = -10$ V. $V_{DD} = 15$ V.

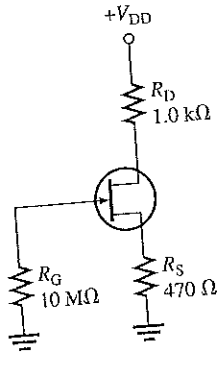
Open the Multisim file E07-09 in the Examples folder on your CD-ROM. The circuit has the calculated values for R_D and R_S from the Related Problem. Verify that an approximate midpoint bias is established by measuring V_D and I_D.

Graphical Analysis of a Self-Biased JFET

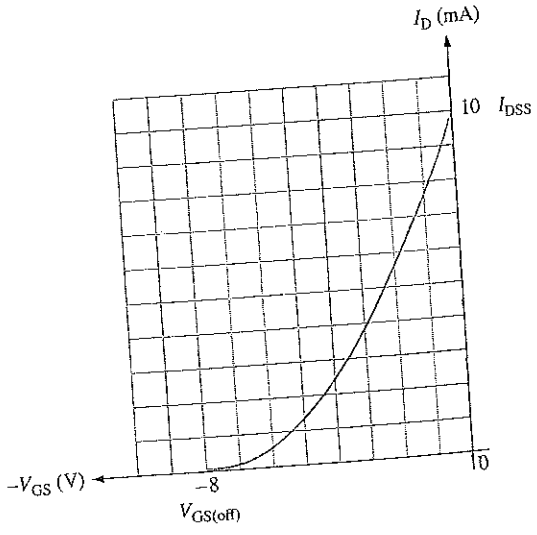
You can use the transfer characteristic curve of a JFET and certain parameters to determine the Q-point (I_D and V_{GS}) of a self-biased circuit. A circuit is shown in Figure 7–20(a), and a transfer characteristic curve is shown in Figure 7–20(b). If a curve is not available from a data sheet, you can plot it from Equation 7–1 using data sheet values for I_{DSS} and $V_{GS(off)}$.

FIGURE 7–20

A self-biased JFET and its transfer characteristic curve.



(a)



(b)

To determine the Q-point of the circuit in Figure 7–20(a), a self-bias dc load line is established on the graph in part (b) as follows. First, calculate V_{GS} when I_D is zero.

$$V_{GS} = -I_D R_S = (0)\,(470\ \Omega) = 0\ \text{V}$$

This establishes a point at the origin on the graph ($I_D = 0$, $V_{GS} = 0$). Next, calculate V_{GS} when $I_D = I_{DSS}$. From the curve in Figure 7–20(b), $I_{DSS} = 10$ mA.

$$V_{GS} = -I_D R_S = -(10\ \text{mA})\,(470\ \Omega) = -4.7\ \text{V}$$

This establishes a second point on the graph ($I_D = 10$ mA, $V_{GS} = -4.7$ V). Now, with two points, the load line can be drawn on the transfer characteristic curve as shown in Figure 7–21. The point where the line intersects the transfer characteristic curve is the Q-point of the circuit as shown.

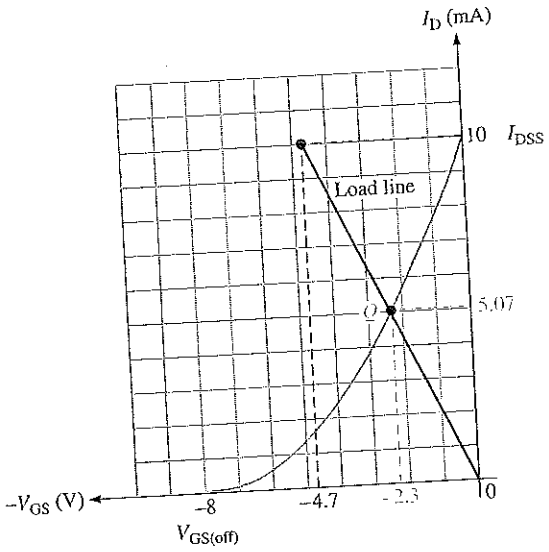
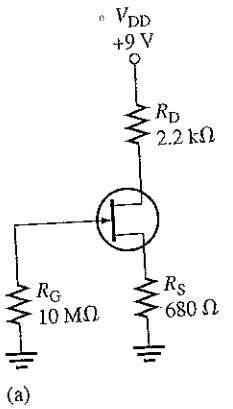


FIGURE 7–21
The intersection of the self-bias dc load line and the transfer characteristic curve is the Q-point.

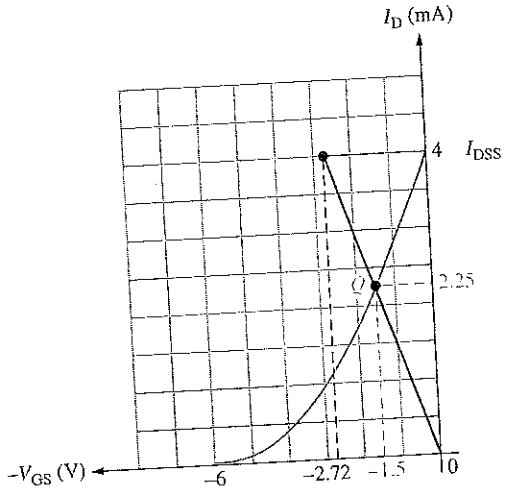
EXAMPLE 7–10

Determine the Q-point for the JFET circuit in Figure 7–22(a). The transfer characteristic curve is given in Figure 7–22(b).

FIGURE 7–22



(a)



(b)

Solution For $I_D = 0$,

$$V_{GS} = -I_D R_S = (0)(680\ \Omega) = 0\ \text{V}$$

This gives a point at the origin. From the curve, $I_{DSS} = 4$ mA; so $I_D = I_{DSS} = 4$ mA.

$$V_{GS} = -I_D R_S = -(4\ \text{mA})(680\ \Omega) = -2.72\ \text{V}$$

This gives a second point at 4 mA and −2.72 V. A line is now drawn between the two points, and the values of I_D and V_{GS} at the intersection of the line and the curve are taken from the graph, as illustrated in Figure 7–22(b). The Q-point values from the graph are

$$I_D = \mathbf{2.25\ mA}$$
$$V_{GS} = \mathbf{-1.5\ V}$$

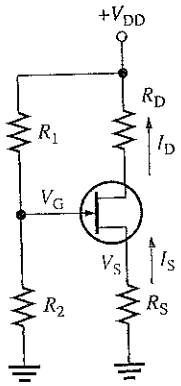
Related Problem If R_S is increased to 1.0 kΩ in Figure 7–22(a), what is the new Q-point?

Voltage-Divider Bias

An *n*-channel JFET with voltage-divider bias is shown in Figure 7–23. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

FIGURE 7–23

An *n*-channel JFET with voltage-divider bias ($I_S = I_D$).



The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

and the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

$$I_D = \frac{V_S}{R_S}$$

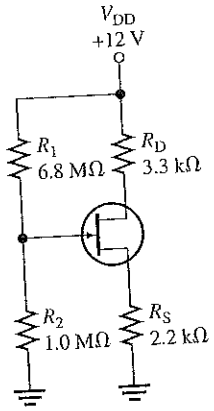
Substituting for V_S,

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

EXAMPLE 7–11

Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 7–24, given that for this particular JFET the internal parameter values are such that $V_D \cong 7$ V.

FIGURE 7–24



Solution

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52\text{ mA})(2.2\text{ k}\Omega) = 3.34\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{1.0\text{ M}\Omega}{7.8\text{ M}\Omega}\right)12\text{ V} = 1.54\text{ V}$$

$$V_{GS} = V_G - V_S = 1.54\text{ V} - 3.34\text{ V} = \mathbf{-1.8\text{ V}}$$

If V_D had not been given in this example, the Q-point values could not have been found without the transfer characteristic curve.

Related Problem Given that $V_D = 6$ V when another JFET is inserted in the circuit of Figure 7–24, determine the Q-point.

Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.

In a JFET with voltage-divider bias when $I_D = 0$, V_{GS} is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For $I_D = 0$,

$$V_S = I_D R_S = (0)R_S = 0\text{ V}$$
$$V_{GS} = V_G - V_S = V_G - 0\text{ V} = V_G$$

Therefore, one point on the line is at $I_D = 0$ and $V_{GS} = V_G$.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at $I_D = V_G/R_S$ and $V_{GS} = 0$. The generalized dc load line is shown in Figure 7–25. The point at which the load line intersects the transfer characteristic curve is the Q-point.

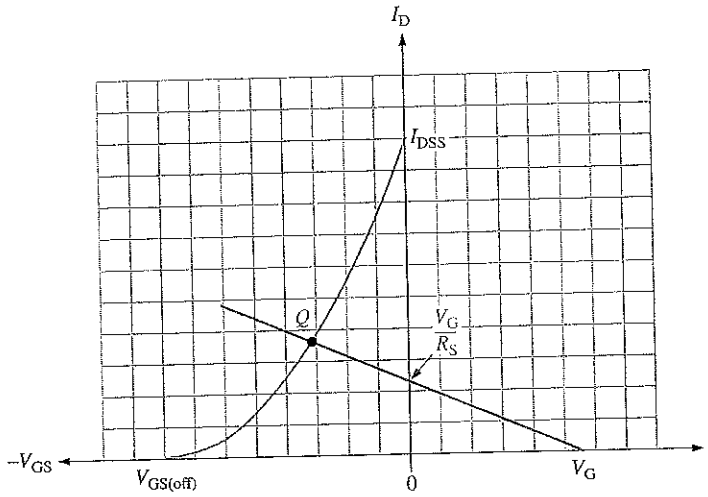


FIGURE 7–25
Generalized dc load line for a JFET with voltage-divider bias.

EXAMPLE 7–12

Determine the approximate Q-point for the JFET with voltage-divider bias in Figure 7–26(a), given that this particular device has a transfer characteristic curve as shown in Figure 7–26(b).

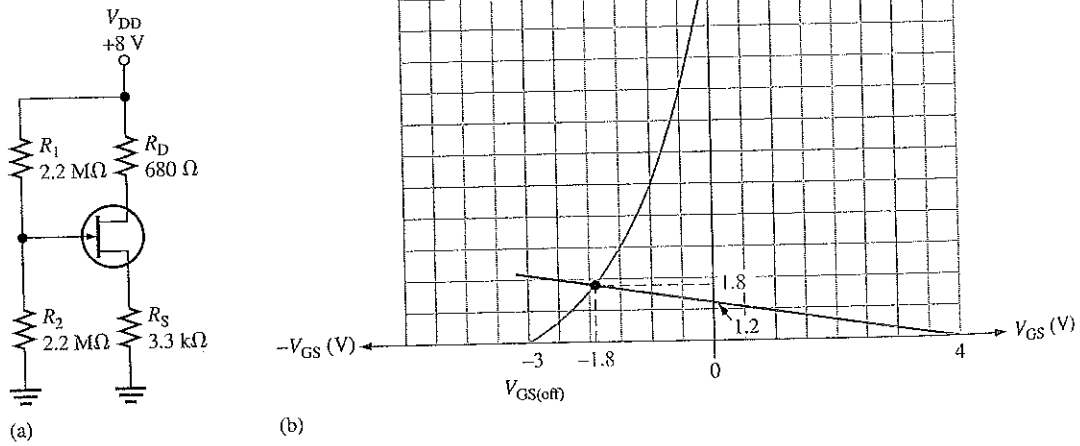


FIGURE 7–26

Solution First, establish the two points for the bias line. For $I_D = 0$,

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{2.2\ \text{M}\Omega}{4.4\ \text{M}\Omega}\right)8\ \text{V} = 4\ \text{V}$$

The first point is at $I_D = 0$ and $V_{GS} = 4$ V. For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} = \frac{4\ \text{V}}{3.3\ \text{k}\Omega} = 1.2\ \text{mA}$$

The second point is at $I_D = 1.2$ mA and $V_{GS} = 0$.

The load line is drawn in Figure 7–26(b), and the approximate Q-point values of $I_D \cong \mathbf{1.8\ mA}$ and $V_{GS} \cong \mathbf{-1.8\ V}$ are picked off the graph, as indicated.

Related Problem Change R_S to 4.7 kΩ and determine the Q-point for the circuit in Figure 7–26(a).

Open the Multisim file E07-12 in the Examples folder on your CD-ROM. Measure the Q-point values of I_D and V_{GS} and see how they compare to the graphically determined values from the Related Problem.

Q-Point Stability

Unfortunately, the transfer characteristic of a JFET can differ considerably from one device to another of the same type. If, for example, a 2N5459 JFET is replaced in a given bias circuit with another 2N5459, the transfer characteristic curve can vary greatly, as illustrated in Figure 7–27(a). In this case, the maximum I_{DSS} is 16 mA and the minimum I_{DSS} is 4 mA. Likewise, the maximum $V_{GS(off)}$ is -8 V and the minimum $V_{GS(off)}$ is -2 V. This means that if you have a selection of 2N5459s and you randomly pick one out, it can have values anywhere within these ranges.

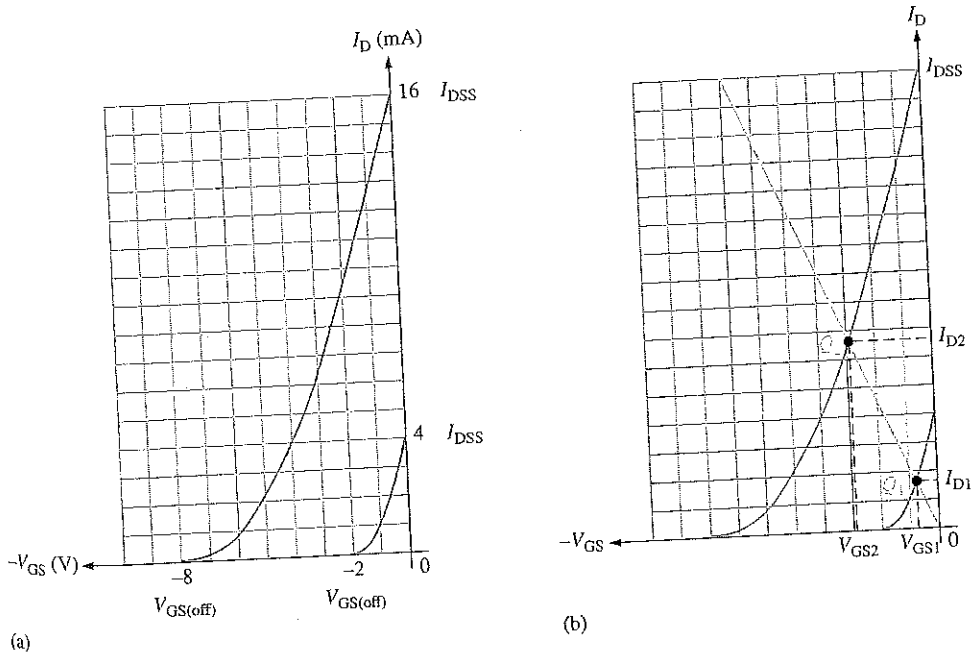


FIGURE 7–27

Variation in the transfer characteristic of 2N5459 JFETs and the effect on the Q-point.

If a self-bias dc load line is drawn as illustrated in Figure 7–27(b), the same circuit using a 2N5459 can have a Q-point anywhere along the line from Q_1, the minimum bias point, to Q_2, the maximum bias point. Accordingly, the drain current can be any value between I_{D1} and I_{D2}, as shown by the shaded area. This means that the dc voltage at the drain can have a range of values depending on I_D. Also, the gate-to-source voltage can be any value between V_{GS1} and V_{GS2}, as indicated.

Figure 7–28 illustrates Q-point stability for a self-biased JFET and for a JFET with voltage-divider bias. With voltage-divider bias, the dependency of I_D on the range of Q-points is reduced because the slope of the bias line is less than for self-bias for a given JFET. Although V_{GS} varies quite a bit for both self-bias and voltage-divider bias, I_D is much more stable with voltage-divider bias.

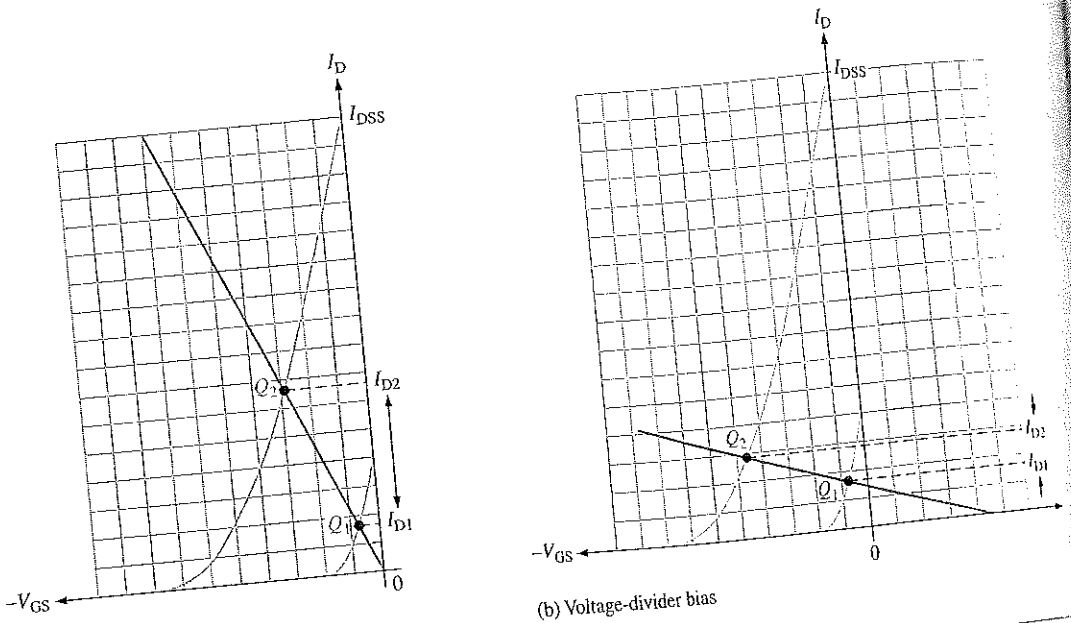


FIGURE 7–28

The change in I_D between the minimum and the maximum Q-points is much less for a JFET with voltage-divider bias than for a self-biased JFET.

SECTION 7–3 REVIEW

1. Should a *p*-channel JFET have a positive or a negative V_{GS}?
2. In a certain self-biased *n*-channel JFET circuit, $I_D = 8$ mA and $R_S = 1.0$ kΩ. Determine V_{GS}.
3. An *n*-channel JFET with voltage-divider bias has a gate voltage of 3 V and a source voltage of 5 V. Calculate V_{GS}.

7–4 THE MOSFET

The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET differs from the JFET in that it has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are

depletion (D) and enhancement (E). Because of the insulated gate, these devices are sometimes called IGFETs.

After completing this section, you should be able to

- **Explain the operation of MOSFETs**
- Describe the structural difference between an *n*-channel and a *p*-channel depletion MOSFET (D-MOSFET)
- Explain the depletion mode
- Explain the enhancement mode
- Identify the symbols for *n*-channel and *p*-channel D-MOSFETs
- Describe the structural difference between an *n*-channel and a *p*-channel enhancement MOSFET (E-MOSFET)
- Identify the symbols for *n*-channel and *p*-channel E-MOSFETs
- Explain how D-MOSFETs and E-MOSFETs differ
- Discuss power MOSFETs
- Discuss dual-gate MOSFETs

Depletion MOSFET (D-MOSFET)

One type of **MOSFET** is the depletion MOSFET (D-MOSFET), and Figure 7–29 illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both *n*-channel and *p*-channel devices are shown in the figure. We will use the *n*-channel device to describe the basic operation. The *p*-channel operation is the same, except the voltage polarities are opposite those of the *n*-channel.

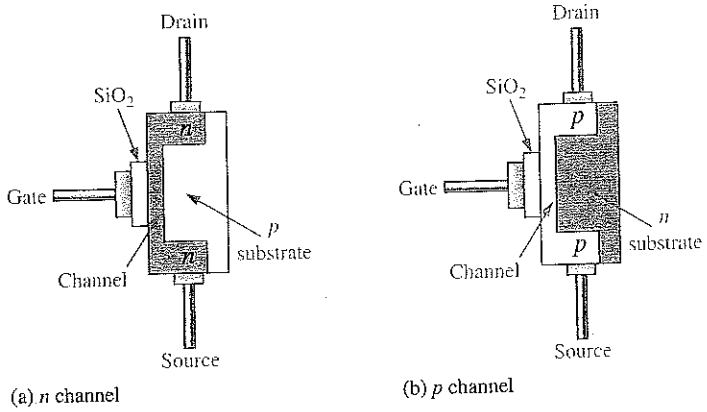
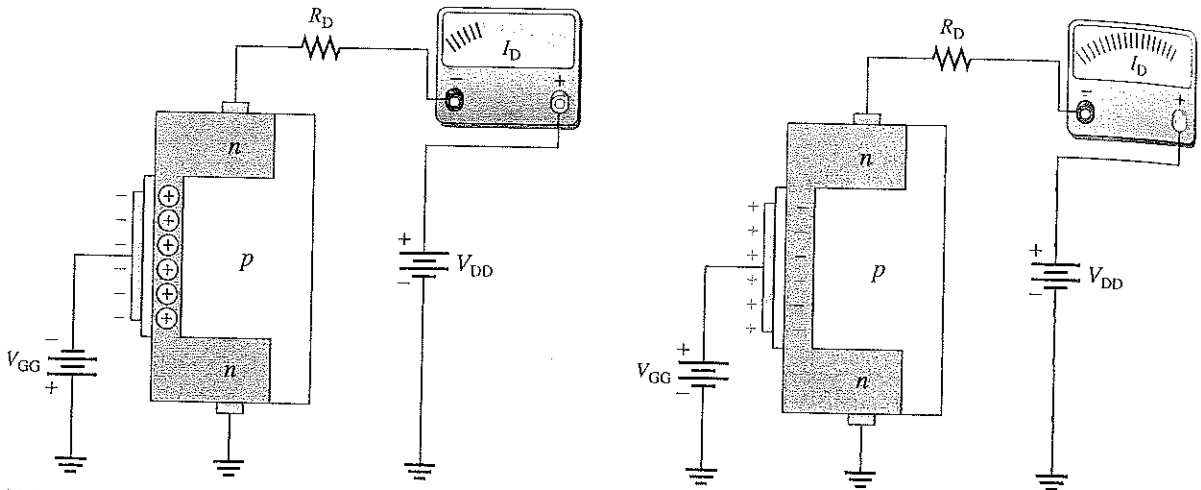


FIGURE 7–29
Representation of the basic structure of D-MOSFETs.

The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode—and is sometimes called a *depletion/enhancement MOSFET.* Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The *n*-channel MOSFET operates in the **depletion** mode when a negative gate-to-source voltage is applied and in the **enhancement** mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.

Depletion Mode Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the *n* channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of *n*-channel electrons. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure 7–30(a). Like the *n*-channel JFET, the *n*-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.



(a) Depletion mode: V_{GS} negative and less than $V_{GS(off)}$

(b) Enhancement mode: V_{GS} positive

FIGURE 7–30

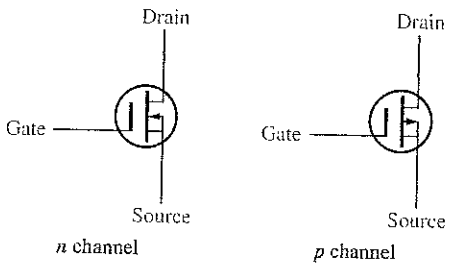
Operation of *n*-channel D-MOSFET.

Enhancement Mode With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure 7–30(b).

D-MOSFET Symbols The schematic symbols for both the *n*-channel and the *p*-channel depletion MOSFETs are shown in Figure 7–31. The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin. An inward-pointing substrate arrow is for *n* channel, and an outward-pointing arrow is for *p* channel.

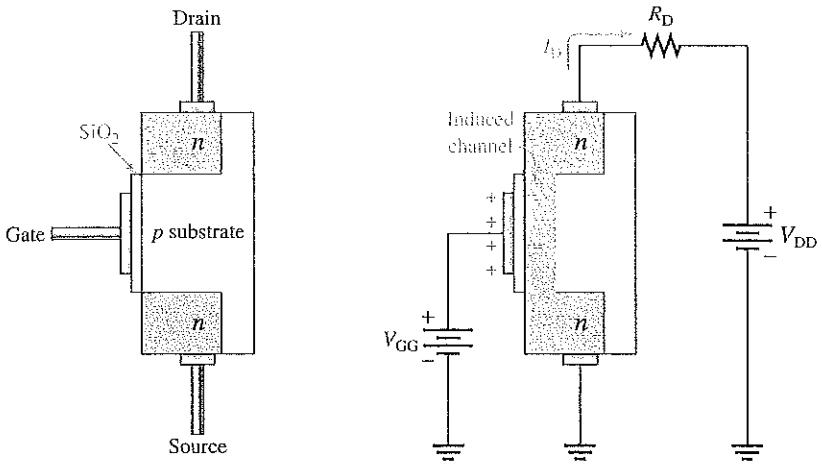
FIGURE 7–31

D-MOSFET schematic symbols.



Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates *only* in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET in that it has no structural channel. Notice in Figure 7–32(a) that the substrate extends completely to the SiO_2 layer. For an *n*-channel device, a positive gate voltage above a threshold value *induces* a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure 7–32(b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.



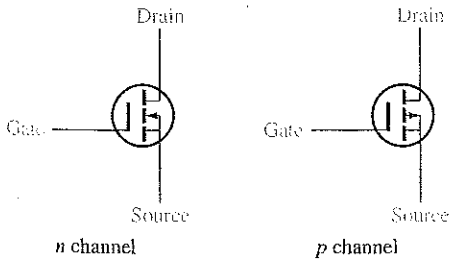
(a) Basic construction

(b) Induced channel ($V_{GS} > V_{GS(th)}$)

FIGURE 7–32

Representation of the basic E-MOSFET construction and operation (*n*-channel).

The schematic symbols for the *n*-channel and *p*-channel E-MOSFETs are shown in Figure 7–33. The broken lines symbolize the absence of a physical channel. Like the D-MOSFET, some devices have a separate substrate connection.



n channel *p* channel

FIGURE 7–33

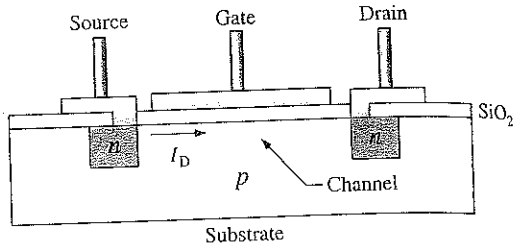
E-MOSFET schematic symbols.

Power MOSFETs

The conventional enhancement MOSFETs have a long thin lateral channel as shown in the structural view in Figure 7–34. This results in a relatively high drain-to-source resistance and limits the E-MOSFET to low power applications. When the gate is positive, the channel is formed close to the gate between the source and the drain, as shown.

FIGURE 7–34

Cross section of conventional E-MOSFET structure. Channel is shown as white area.

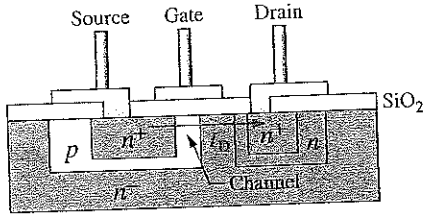


Lateral Double Diffused MOSFET (LDMOSFET) The LDMOSFET is a type of enhancement MOSFET designed for power applications. This device has a shorter channel between drain and source than does the conventional E-MOSFET. The shorter channel results in lower resistance, which allows higher current and voltage.

Figure 7–35 shows the basic structure of an LDMOSFET. When the gate is positive, a very short n channel is induced in the p layer between the lightly doped source and the n^- region. There is current to the drain through the n regions and the induced channel from the source, as indicated.

FIGURE 7–35

Cross section of LDMOSFET structure.

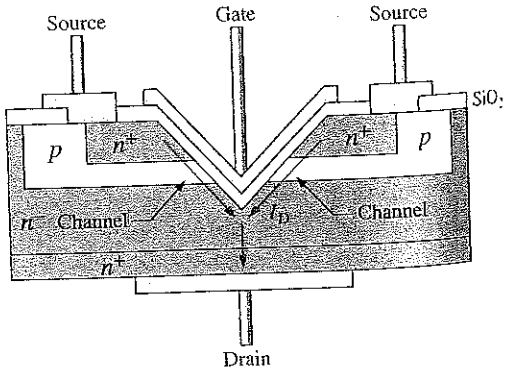


VMOSFET The V-groove MOSFET is another variation of the conventional E-MOSFET designed to achieve higher power capability by creating a shorter and wider channel with less resistance between the drain and source. The shorter, wider channels allow for higher currents and, thus, greater power dissipation. Frequency response is also improved.

The VMOSFET has two source connections, a gate connection on top, and a drain connection on the bottom, as shown in Figure 7–36. The channel is induced vertically along both sides of the V-shaped groove between the drain (n^+ substrate where n^+ means a higher doping level than n^-) and the source connections. The channel length is set by the thickness of the layers, which is controlled by doping densities and diffusion time rather than by mask dimensions.

FIGURE 7–36

Cross section of VMOSFET structure.



TMOSFET TMOSFET is similar to VMOSFET except that it doesn't use a V-shaped groove and is, therefore, easier to manufacture. The structure of TMOSFET is illustrated in Figure 7–37. The gate structure is embedded in a silicon dioxide layer, and the source con-

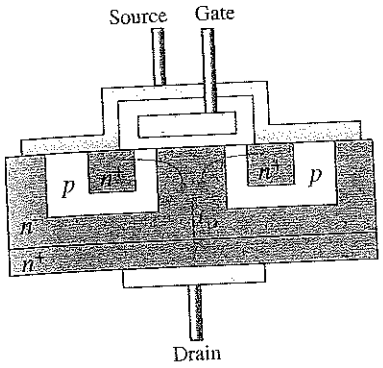


FIGURE 7–37
Cross section of TMOSFET structure.

fact is continuous over the entire surface area. The drain is on the bottom. TMOSFET achieves greater packing density than VMOSFET, while retaining the short vertical channel advantage.

Dual-Gate MOSFETs

The dual-gate MOSFET can be either a depletion or an enhancement type. The only difference is that it has two gates, as shown in Figure 7–38. As previously mentioned, one drawback of a FET is its high input capacitance, which restricts its use at higher frequencies. By using a dual-gate device, the input capacitance is reduced, thus making the device useful in high-frequency RF amplifier applications. Another advantage of the dual-gate arrangement is that it allows for an automatic gain control (AGC) input in certain RF amplifiers.

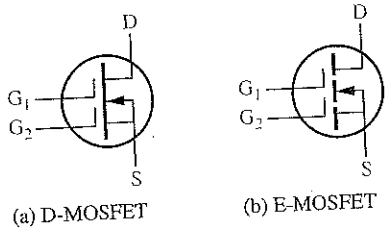


FIGURE 7–38
Dual-gate *n*-channel MOSFET symbols.

SECTION 7–4 REVIEW

1. Name the two basic types of MOSFETs.
2. If the gate-to-source voltage in an *n*-channel depletion MOSFET is made more negative, does the drain current increase or decrease?
3. If the gate-to-source voltage in an *n*-channel E-MOSFET is made more positive, does the drain current increase or decrease?

7–5 MOSFET CHARACTERISTICS AND PARAMETERS

Much of the discussion concerning JFET characteristics and parameters applies equally to MOSFETs. In this section, MOSFET parameters are discussed.

After completing this section, you should be able to

- **Define, discuss, and apply important MOSFET parameters**
- Analyze a D-MOSFET transfer characteristic curve

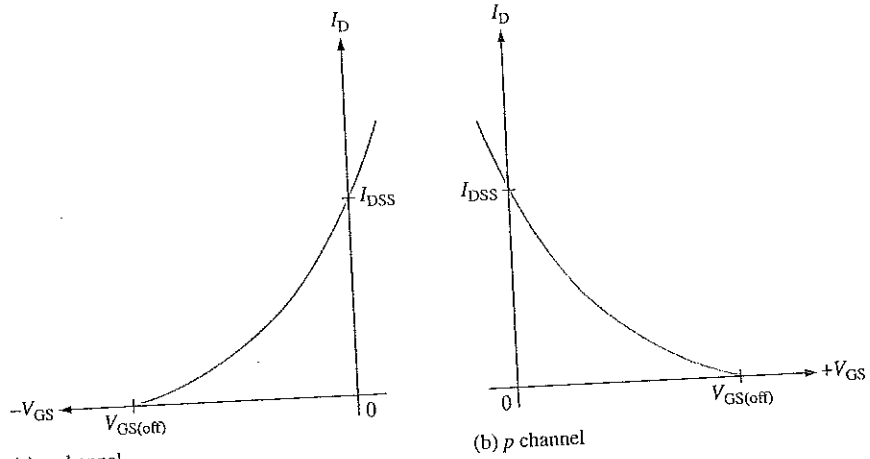
- Use the equation for the D-MOSFET transfer characteristic to calculate I_D
- Analyze an E-MOSFET transfer characteristic curve
- Use the equation for the E-MOSFET transfer characteristic to calculate I_D
- Use a MOSFET data sheet
- Discuss handling precautions for MOS devices

D-MOSFET Transfer Characteristic

As previously discussed, the D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure 7–39 for both *n*-channel and *p*-channel MOSFETs. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_P$.

The square-law expression in Equation 7–1 for the JFET curve also applies to the D-MOSFET curve, as Example 7–13 demonstrates.

FIGURE 7–39
D-MOSFET general transfer characteristic curves.



EXAMPLE 7–13

For a certain D-MOSFET, $I_{DSS} = 10$ mA and $V_{GS(off)} = -8$ V.

(a) Is this an *n*-channel or a *p*-channel?

(b) Calculate I_D at $V_{GS} = -3$ V.

(c) Calculate I_D at $V_{GS} = +3$ V.

Solution

(a) The device has a negative $V_{GS(off)}$; therefore, it is an ***n*-channel** MOSFET.

(b) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left(1 - \frac{-3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{3.91\text{ mA}}$$

(c) $$I_D = (10\text{ mA})\left(1 - \frac{+3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{18.9\text{ mA}}$$

Related Problem For a certain D-MOSFET, $I_{DSS} = 18$ mA and $V_{GS(off)} = +10$ V.

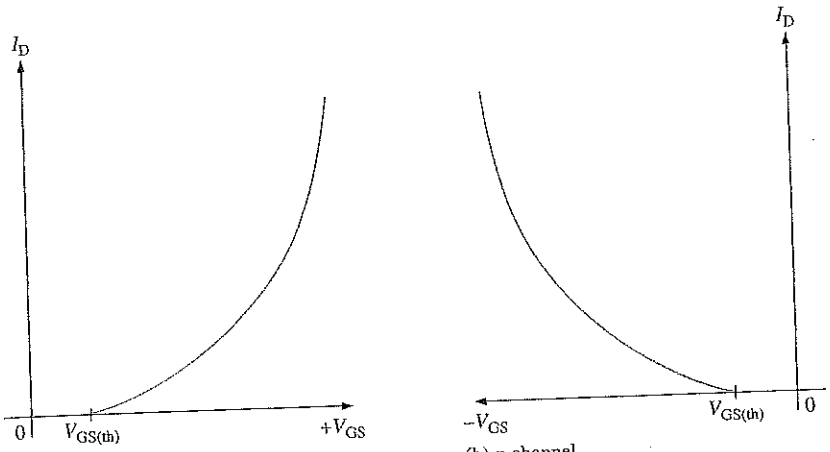
(a) Is this an *n*-channel or a *p*-channel?

(b) Determine I_D at $V_{GS} = +4$ V.

(c) Determine I_D at $V_{GS} = -4$ V.

E-MOSFET Transfer Characteristic

The E-MOSFET uses only channel enhancement. Therefore, an *n*-channel device requires a positive gate-to-source voltage, and a *p*-channel device requires a negative gate-to-source voltage. Figure 7–40 shows the general transfer characteristic curves for both types of E-MOSFETs. As you can see, there is no drain current when $V_{GS} = 0$. Therefore, the E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET. Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the *threshold voltage*, $V_{GS(th)}$.



(a) *n* channel (b) *p* channel

FIGURE 7–40
E-MOSFET general transfer characteristic curves.

The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E-MOSFET transfer characteristic curve is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$ **Equation 7–4**

The constant K depends on the particular MOSFET and can be determined from the data sheet by taking the specified value of I_D, called $I_{D(on)}$, at the given value of V_{GS} and substituting the values into Equation 7–4. A typical E-MOSFET data sheet is given in Figure 7–41.

EXAMPLE 7–14

The data sheet in Figure 7–41 for a 2N7008 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

Solution First, solve for K using Equation 7–4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500 \text{ mA}}{(10 \text{ V} - 1 \text{ V})^2} = \frac{500 \text{ mA}}{81 \text{ V}^2} = 6.17 \text{ mA/V}^2$$

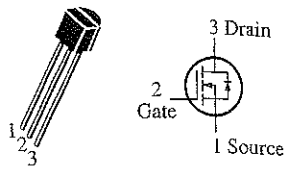
Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17 \text{ mA/V}^2)(5 \text{ V} - 1 \text{ V})^2 = \mathbf{98.7 \text{ mA}}$$

Related Problem The data sheet for an E-MOSFET gives $I_{D(on)} = 100$ mA at $V_{GS} = 8$ V and $V_{GS(th)} = 4$ V. Find I_D when $V_{GS} = 6$ V.

2N7008

Case 29-04, Style 22
TO-92 (TO-226AA)



TMOS FET Transistor

N channel — Enhancement

Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DSS}	60	V dc
Drain-Gate voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	V dc
Gate-Source voltage	V_{GS}	±40	V dc
Drain current Continuous Pulsed	 I_D I_{DM}	 150 1000	mA dc
Total power dissipation @ T_A = 25°C Derate above 25°C	P_D	400 3.2	mW mW/°C
Operating and storage temperature range	T_J, T_{stg}	−55 to +150	°C

Thermal Characteristics

Thermal resistance junction to ambient	$R_{\theta JA}$	312.5	°C/W
Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	T_L	300	°C

Electrical Characteristics (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF Characteristics				
Drain-Source breakdown voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	–	V dc
Zero gate voltage drain current (V_{DS} = 50 V, V_{GS} = 0) (V_{DS} = 50 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	– –	1.0 500	μA dc
Gate-Body leakage current, forward (V_{GSF} = 30 V dc, V_{DS} = 0)	I_{GSSF}	–	−100	nA dc
ON Characteristics				
Gate threshold voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	1.0	2.5	V dc
Static drain-source on-resistance (V_{GS} = 5.0 V dc, I_D = 50 A dc) (V_{GS} = 10 V dc, I_D = 500 mA dc, T_C = 125°C)	$r_{DS(on)}$	– –	7.5 13.5	Ohm
Drain-Source on-voltage (V_{GS} = 5.0 V, I_D = 50 mA) (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$	– –	1.5 3.75	V dc
On-state drain current (V_{GS} = 10 V, $V_{DS} \geq 2.0V_{D(on)}$)	$I_{D(on)}$	500	–	mA
Forward transconductance ($V_{DS} \geq 2.0V_{DS(on)}$, I_D = 200 mA)	g_{fs}	80	–	μmhos or μS
Dynamic Characteristics				
Input capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	–	50	pF
Output capacitance		C_{oss}	–	25	
Reverse transfer capacitance		C_{rss}	–	5.0	
Switching Characteristics				
Turn-On delay time	(V_{DD} = 30 V, I_D = 200 mA R_{gen} = 25 ohms, R_L = 150 ohms)	t_{on}	–	20	ns
Turn-Off delay time		t_{off}	–	20	

FIGURE 7-41

Data sheet for the 2N7008 *n*-channel E-MOSFET (TMOSFET construction).

Handling Precautions

All MOS devices are subject to damage from electrostatic discharge (ESD). Because the gate of a MOSFET is insulated from the channel, the input resistance is extremely high (ideally infinite). The gate leakage current, I_{GSS}, for a typical MOSFET is in the pA range, whereas the gate reverse current for a typical JFET is in the nA range. The input capacitance results from the insulated gate structure. Excess static charge can be accumulated because the input capacitance combines with the very high input resistance and can result in damage to the device. To avoid damage from ESD, certain precautions should be taken when handling MOSFETs:

1. MOS devices should be shipped and stored in conductive foam.
2. All instruments and metal benches used in assembly or test should be connected to earth ground (round or third prong of 110 V wall outlets).

3. The assembler's or handler's wrist should be connected to earth ground with a length of wire and a high-value series resistor.
4. Never remove a MOS device (or any other device, for that matter) from the circuit while the power is on.
5. Do not apply signals to a MOS device while the dc power supply is off.

SECTION 7–5 REVIEW

1. What is the major difference in construction of the D-MOSFET and the E-MOSFET?
2. Name two parameters of an E-MOSFET that are not specified for D-MOSFETs?
3. What is ESD?

7–6 MOSFET BIASING

Three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias. Biasing is important in FET amplifiers, which you will study in the next chapter.

After completing this section, you should be able to

- **Discuss and analyze MOSFET bias circuits**
- Describe zero-bias of a D-MOSFET
- Analyze a zero-biased MOSFET circuit
- Describe voltage-divider bias of an E-MOSFET
- Describe drain-feedback bias of an E-MOSFET

D-MOSFET Bias

Recall that D-MOSFETs can be operated with either positive or negative values of V_{GS}. A simple bias method is to set $V_{GS} = 0$ so that an ac signal at the gate varies the gate-to-source voltage above and below this 0 V bias point. A MOSFET with zero bias is shown in Figure 7–42(a). Since $V_{GS} = 0$, $I_D = I_{DSS}$ as indicated. The drain-to-source voltage is expressed as follows:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The purpose of R_G is to accommodate an ac signal input by isolating it from ground, as shown in Figure 7–42(b). Since there is no dc gate current, R_G does not affect the zero gate-to-source bias.

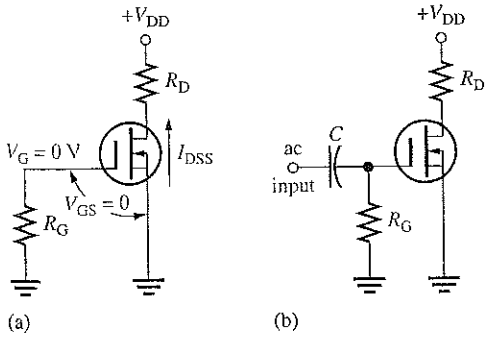


FIGURE 7–42
A zero-biased D-MOSFET.